ABSTRACT OF THE DISCLOSURE

A SYNC pulse compensation and regeneration apparatus and method for use with a high skew tolerant, low latency clock synchronizer controller utilized for synchronizing data transfer operations between two circuit portions across a clock domain boundary. A primary clock signal is operable to clock a first circuit portion and a secondary clock signal, generated from the primary clock signal, is operable to clock a second circuit portion. A SYNC pulse signal is generated based on coincident rising edges of the primary and secondary clock signals. A sampling compensation circuit is operable to condition the SYNC pulse signal by inserting a logic high pulse when the SYNC pulse is lost, or by removing duplicate SYNC pulses when necessary. A jitter cycle delay compensation circuit coupled to the sampling compensation circuit is operable to stage the SYNC pulse through a series of delay registers to compensate for clock skew when the SYNC pulse jumps ahead or behind a clock cycle.